Nigerian Journal of Applied Physics (NJAP)
ISSN Print: 3115-5871
ISSN Online: 3115-588X
DOI: https://doi.org/10.62292/njap-v2i1-2026-55
Volume 2(1), March 2026

Evaluation of CNTFETs Temperatures and their Performance using High-K Gate Dielectrics to Enhance Nanoelectronic Applications

***[1]Maryam Ibrahim and [2]Garba Shehu M. Galadanci**

[1]Department of Physics, Northwest University Kano, Kano State, Nigeria
[2]Department of Physics, Bayero University Kano State, Nigeria.

*Corresponding author's email: maryambnibrahim@gmail.com

ABSTRACT

High-k dielectrics combined with CNTFETs are potential alternative to next-generation nanoelectronics devices when the traditional silicon-based devices are nearing a scaling limit due to increasing leakage current and power dissipation. The performance of Carbon Nanotube Field Effect Transistors (CNTFETs) is examined in this work in relation to temperature change and high-k dielectric constants (high-k gate materials). This paper employed the cylindrical CNTFET model as a tool to examine six dielectric materials, namely SiO_2,Al_2O_3,Y_2O_3,Ta_2O_5,HfO_2, and La_2O_3 at wide temperature range of 300 K to 1000 K. The key performance parameters that are investigated, include ON current, OFF current, subthreshold swing (SS), drain induced barrier lowering (DIBL), transconductance (gm), output conductance (gd), voltage gain (A_V), and carrier injunction velocity (V_{inj}). The results show that increasing dielectric constant enhances the ON current, transconductance, and carrier injection velocity due to an improved gate capacitance and a stronger electrostatic control. On the other hand, higher temperatures cause subthreshold swing to deteriorate and OFF current to increase, showing decreased switching efficiency under high thermal circumstances. At 1000 K, La_2O_3 outperformed lower-k materials in terms of drive current (7.775e-05A) and carrier transport (6.042e+05m/s). The research also indicates that temperature affects significantly short-channel effects such as DIBL and leakage behavior. As much as the thermal effects need to be put under control to achieve maximum reliable and efficient devices, the integration of high-k dielectrics and CNTFET architectures have immense potential in providing high-performance and low-power applications.

Keywords:
Carbon Nanotube Field Effect Transistors (CNTFETs), Transconductance (gm), Subthreshold swing (SS), High-k dielectric materials, Nanoelectronics.

INTRODUCTION

Semiconductor nanostructures are currently of immense interest and significance to the research community, owing to their distinctive nature and interdisciplinary applications in areas such as nanoelectronics. They are also being considered as potential building blocks of post-CMOS devices in order to facilitate scaling of the devices (*Talin, 2018*). The motivation behind this trend is that smaller transistors will allow the integration of more complex processors and an increasing number of their components per unit area, faster switching speed and, by extension, reduced processing times. But, as the dimensions of a typical transistor are limited on a fundamental basis, there are some restrictions on this kind of shrinking (*Yacobi, 2004*). Small, light, low power, high performance, and feature-enhanced electronic devices are highly demanded (*Dass et al, 2013)*. The decline in the cost-per-function has continued to increase the economic productivity of every succeeding generation of technology. CMOS transistors have now become the main material of integrated circuits (ICs) since they are scalable, and have some special properties of devices, most notably high input resistance, self-isolation, zero dissipation of static power, and an easy designing and fabrication process. CMOS ICs are ubiquitous and indispensably found in all aspects of transportation and telecommunications to portable devices these days *(Kim, 2010*). The exponential increase in the gate-dielectric leakage current has, as expected, caused and continues to cause serious concerns regarding the operation of CMOS devices, particularly with regard to power dissipation in standby operations, life-span, and the reliability of CMOS

devices. This exponential dependence of gate leakage current on dielectric thickness is likely to be one of the causes, although not the only ones, of the limited extendibility of SiO_2 as a gate dielectric (*Buchanan, 1999*). The thickness of silicon dioxide gate dielectric has been slowly reduced with transistors becoming smaller in size so as to increase the drive current and improve gate capacitance to enhance the performance of devices. Tunneling leakage is dramatically larger with a thickness below 1.5 nm leading to excessive power dissipation and reducing device reliability. To circumvent these limitations, there are several options that are erected. Others include modifying the existing technologies and arrangements with expectations of enhancing their scalability. The other alternatives would be to substitute the existing silicon MOSFETs with new materials and technologies. Scientists are currently focusing on identifying the alternatives that would enable the electronics systems to keep on performing better. Such alternatives are metal gate electrodes, dual gate FETs and high dielectric constant (High-K) insulating material. High-K dielectric materials are desirable in gate insulators since they can be used effectively to inject charge into transistor channels and reduce the direct tunneling leakage currents (*Sinha & Chaudhury, 2012*). Replacing silicon dioxide gate dielectric with High-k material can increase gate capacitance without the leakage effects (*Dass et al.*, 2013).

Carbon nanotubes (CNT) are often considered the most promising candidates to replace silicon technology as silicon-based technology is limited by scaling challenges that impede the development of transistor technology. Carbon nanotube field effect transistors (CNTFETs) are considered to be the most promising devices with some outstanding features, such as high current carrying capacity (~1010 A/cm 2), high carrier mobility, scalability, high reliability in high temperature, and low leakage current (*Kumari et al., 2019*). Electrical and thermal transport in metallic single-walled carbon nanotubes (SWCNTs) on an insulating substrate are investigated, and this suggests that the self-heating effect may lead to rise in temperature in the SWCNTs. The temperature increase of the semiconducting CNT channel is observed to be much lower than that of the metallic counterpart *(Xing et al., 2011)*. The nature and behavior of MOSFET devices that also change with changes in temperature were also investigated, temperature plays a significant role that affects the performance and features of CNTFETs (*Naderi et al., 2012*). *(Dixit & Gupta, 2020)* presented the analysis of carbon nanotube field effect transistors (CNFETs) using various high-k gate dielectric materials. In their findings they reported that as thickness of gate dielectric material reduces, drain current of CNFET increases very marginally. Temperature variation effects on carbon nanotube field effect transistor were also analyzed using Nano electronics device simulating software *by (Tijjani et al., 2022)* it was shown in their result that, there is no appreciable variation for change in temperature. The variation of the alternating current (ac) conductivity, dielectric constant (k), dielectric loss, impedance (Z) and electric modulus were studied as a function of frequency and temperature by *(Hegde et al., 2024)*. Their results showed that the dielectric properties and ac conductivity of the prepared nanoparticles were dependent on frequency and temperature. The impact of temperature and dielectric constant to evaluate the input–output characteristic of CNTFET devices was evaluated by *(Hossain et al., 2025)* and they reported that the output and input characteristics of a carbon nanotube field-effect transistor (CNTFET) are affected by the device's dielectric materials and operating temperature. However, prior investigations have been reported with different number of dielectric materials, limited performance parameters evaluated and narrow range of temperature (to our knowledge not higher than 600 K) leading to some unsolved fundamental problems associated with the performance.

In this work, we investigate the effects of temperature variation (300 K, 350 K, 400 K, 450 K, 500 K, 550 K, 600 K, 650 K, 700 K, 750 K, 800 K, 850 K, 900 K, 950 K & 1000 K on the performance of carbon nanotube field effect transistor (CNTFET) using various high-k dielectric materials that include; SiO_2, Al_2O_3, Y_2O_3, Ta_2O_5, HfO_2, and La_2O_3 Important performance parameters such as the ON current, Drain induced Barrier Lowering (DIBL), Sub-threshold swing (SS) and transconductance (gm) are evaluated by varying the temperature.

Basic Theory

Structure and operation of MOSFET

The structure of the n-channel MOSFET is reviewed in Figure 1. The figure identifies its n+ type source and drain, p type substrate, channel region, gate conductor and oxide dielectric between the gate and channel.

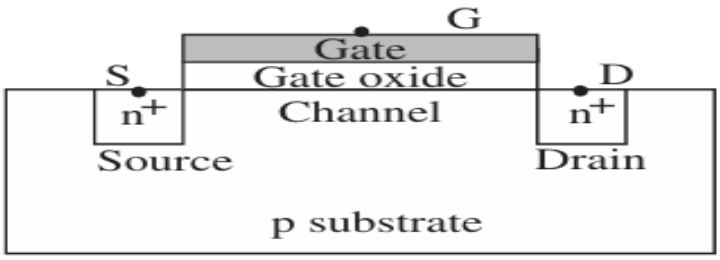

Figure 1: MOSFET structure (*Agarwal & H-Lang., 2005*)

Figure 2 represents the same n-channel MOSFET with source and substrate grounded, the gate and the drain are connected to positive voltages. When the positive gate voltage is applied, the electrons move from the source into the channel and accumulate under the gate. The density of electrons under the gate is so large that it inverts the channel of the p-type silicon to that of n-type silicon when the voltage of the gate increases beyond the threshold voltage of the MOSFET. Consequently, a continuous n-type channel is created between the source and drain in response to the positive drain voltage, permitting the flow of electrons to take place between the source and the drain and hence, current flows from the drain to the source.

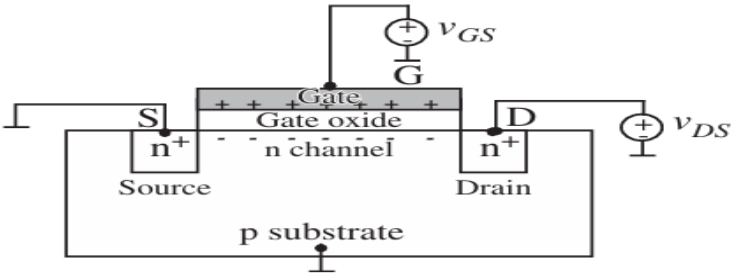

Figure 2: MOSFET with positive voltage applied at the gate relative to the source and substrate (*Agarwal & H-Lang., 2005*)

In Figure 2, the inversion of its channel and activation shows that effectively the MOSFET forms a parallel-plate capacitor between its channel and gate (*Agarwal & H-Lang., 2005*). .

Carbon Nanotubes (CNT) Structure

The carbon nanotubes are the most popular nanostructures. These are highly attractive towards production of electronic components at a level of miniaturization that has never been achieved by silicon technology due to their electrical characteristics (as insulators, semi-conductors or in some cases conductors). As a result, the smallest transistor in the world was developed on the nanometric level (*Nouailhat, 2008*).

Carbon nanotubes can be considered graphene cylinders. Graphene is a sp2-bonded sheet of carbon atoms in single planar sheet as shown in Figure 3. Graphite consists of all of the individual graphene layers deposited over each other. The properties of graphite already give a hint of the exceptional qualities of carbon nanotubes. The charge carrier densities of electrons and holes in graphite are close to each other ($n_e \approx n_h \approx 7X10^{-18}cm^{-3}$), and the measured mobilities are approximately $10^4cm^2V^{-1}s^{-1}$ at ambient temperature and $10^6cm^2V^{-1}s^{-1}$ at 4.2 K *(Hierold, 2008)*.

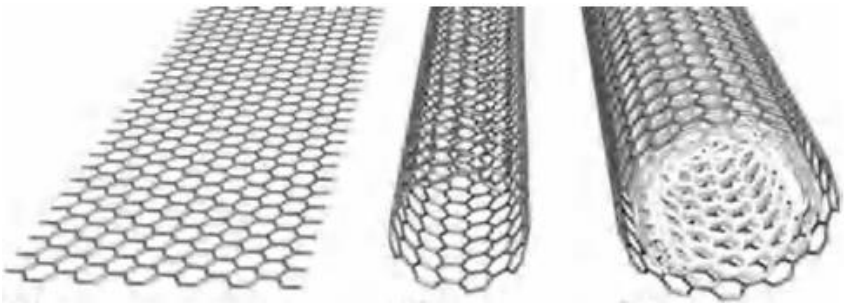

Figure 3: Structure of a single layer of graphite (graphene) (a), single - walled carbon nanotube (b) and a multi-walled carbon nanotube with three shells (c) (*Appenzeller et al., 2002*)

A single-walled carbon nanotube (SWNT) is a graphite roll, with a diameter of 0.5 to a few nanometers, and is either metallic or semiconductor, depending on its chirality. The multi-walled carbon nanotubes (MWNT) are, on the other hand, made of concentric layers of graphene tubes of a few to a hundred nanometers diameter (*Appenzeller et al., 2002*) .

A sheet of graphitic may be rolled into a SWCNT in three forms; some of the nanotubes formed have mirror planes parallel to and perpendicular to the nanotube direction (armchair and zigzag forms). Chiral nanotubes represent the other process of producing CNTs, and does not have mirrors of symmetry as described earlier (*Hornyak et al.*, 2009). Thus, the mathematical definition of the numerous ways in which to roll up graphene into tubes is given by the vector of helicity C_h and the angle of helicity θ.

$$C_h = na_1 + ma_2 \quad (1)$$

$$a_1 = \frac{a\sqrt{3}}{2}x + \frac{a}{2}y \quad and \quad a_2 = \frac{a\sqrt{3}}{2}x - \frac{a}{2}y$$

Where n and m are integers of the vector of helicity considering the unit vectors a_1 and a_2

$$\cos\theta = \frac{2n+m}{2\sqrt{n^2+m^2+nm}} \quad (2)$$

Application of Carbon Nanotubes

Some of the other uses of CNTs that have been reported in numerous literatures include conductive as well as high-strength composites, sensors, energy storage and energy-conversion devices, hydrogen storage media, field emission displays and radiation sources, nanoscale semiconductor devices, probes and interconnects to name a few (*Saleh & Koller, 1991*). The use of nanotubes in biosensors seems more probable. To analyze some compounds, chemists can move them onto biosensors which can bond with other molecules within a given environment. This leads to the manufacture of better detectors. These machines aid in the transportation of medication in the body (*Nouailhat,2008*).

Resistance for SWNTs Circuit Model

When the contacts or the quantum wire contain no scatterings, the lowest possible resistance of a quantum wire is the quantum resistance. The scattering at the contacts results in the contact resistance which can be in hundreds of kilo-ohms in case of inadequate contacts. Electrons flowing down a carbon nanotube (CNT) may be scattered by defects and phonons and their mean free pathways are short. Since the resistance depends on length, nanotubes whose resistance is proportional to length also tend to have large mean free pathways. The observation that nanotubes with a high density of defects have their electrons repeatedly scattered and later lose their phase coherence (*Appenzeller et al., 2002*).

Defects and acoustic phonon backscattering of electrons in SWNTs only occurs at low bias voltage, and in high quality nanotubes, the mean free path length (mfp) of electrons can be as long as 1.6m *(Park et al., 2004*). Greater voltages result in optical and zone-boundary phonons with energies of $\hbar\Omega \approx 0.16$ eV to backscatter electrons (*Javey et al., 2004*). A phonon of energy $\hbar\Omega$ is produced only when a state with energy E− $\hbar\Omega$ is available for an electron with energy E. In order to achieve this energy, an electron has to be propelled by electric field E over a distance of $\ell_\Omega = \hbar\Omega/eE$, where e is the electron charge. Once it has reached this energy, it travels on average ℓ_0 =15 nm before scattering to emit an optical or zone border phonon. The rule of Matthiessen can be used to obtain the effective mfp by giving *(Appenzeller et al., 2002*)

$$\frac{1}{\ell_{eff}} = \frac{1}{\ell_e} + \frac{1}{\ell_\Omega + \ell_o} \quad (3)$$

Where ℓ_e is the low-bias mfp. Resistance of a SWNT is given by *(Appenzeller et al., 2002*)

$$R = R_C + R_Q\left(1 + L/\ell_{eff}\right) \quad (4)$$

Where RC is the contact resistance, and L is the nanotube length.

Capacitance for SWNTs Circuit Model

The Pauli Exclusion Principle states that to provide a quantum wire with electric charge it is necessary to add electrons to accessible states above the Fermi level. The amount of energy required to put an electric charge Q on a quantum wire is (*Appenzeller et al., 2002*).

$$E = \frac{1}{2}\frac{Q^2}{C_E} + \frac{(Q/e)^2}{D(\varepsilon F)} \quad (5)$$

Where e is the charge of the electron and the first term is the energy stored in the electric field (C_E is the electrostatic capacitance). Thus one can define a quantum capacitance in series with an electrostatic capacitance as (*Appenzeller et al., 2002*)

$$C_Q = 2e^2/\left(hv_f\right) \quad (6)$$

Inductance for SWNTs Circuit Model

Whereas magnetic inductance relies solely to the return path distance, kinetic inductance of a SWNT-bundle is inversely proportional to the count of metallic nanotubes. Kinetic and magnetic inductances are summed to give the total inductance *(Appenzeller et al., 2002*).

High-K Gate Dielectric Materials

Any insulating material that has a high dielectric constant (K) that is considerably more than that of silicon dioxide SiO_2, can be called a high-K dielectric. One of the ways of solving the reliability and leakage current issues associated with scaling silicon dioxide may be to use a different insulator, such as a higher permittivity material instead of silicon dioxide (*Demkov et al., 2005)*. The saturated driving current or ON current of a MOSFET can be approximately represented as.

$$I \approx \frac{W}{2L}\mu C\left(V_g - V_t\right)^2 \quad (7)$$

In which W represents transistor width, L represents gate length, μ represents carrier mobility, C represents the

density of the capacitance of the gate insulator, V_g is the gate voltage and V_t is the threshold voltage. The density of the gate insulator capacitance can be estimated as *(Demkov et al., 2005*)

$$C \approx \frac{K\varepsilon_O}{t} \quad (8)$$

Where t is the thickness of the insulator, ε_0 is the permittivity of free space and K is the relative permittivity of the insulator. When a device is scaled, the current of the saturation drive should not change. This means that capacitance should increase with the reduction in the gate voltage and channel length. This increase in capacitance necessitates either increasing K or decreasing t, as we can see from Eq. (8). The common approach has been to decrease the thickness of the insulator. The alternative is to use a so-called high-k material, increase the relative permittivity of the insulator, and hold the insulator thickness. The high-k materials retain the same capacitance density even in cases where they are thicker than SiO_2, This enables the scaled device to store the saturated driving current without the possible leakage and reliability issues of a thinner SiO_2layer *(Demkov et al., 2005*) .

Gate dielectrics with high capacitance, low leakage current, good mechanical flexibility (for use in flexible electronics), and low deposition temperatures are necessary for high performance SWNT TFTs (thin-film transistors, TFTs). The thick oxides are unable to meet those strict standards *(Appenzeller et al., 2002)*.

MATERIALS AND METHODS

The materials and methods employed in the study were covered in this section. This research utilized the Carbon Nanotube Field Effect Transistor (CNTFET) as the channel material with the following six gate dielectric oxides: SiO_2, Al_2O_3, Y_2O_3, Ta_2O_5, HfO_2, and La_2O_3, and FETToy simulator as the software used.

Field Effect Transistor Toy (FETToy)

In this study, the FETToy simulator, a numerical modelling tool designed for ballistic MOSFET simulation, was employed to analyse the performance of CNTFETs. FETToy is a collection of Matlab scripts that computes the ballistic I-V characteristics for conventional MOSFETs, nanowire MOSFETs, and carbon nanotube MOSFETs. FETToy assumes a single or double gate geometry for traditional MOSFETs and a cylindrical geometry for nanowire and nanotube MOSFETs. The simulated device adopts a MOSFET-like architecture with heavily doped source and drain regions. Device operation is governed by barrier height modulation through gate voltage control, where the drain current is determined by the gate-induced charge carriers within the channel *(Nouri-bayat & Kashani-nia, 2017)*.

Modelling

In FETToy software carrier transmission is regarded as ballistic, and the circuit model has two capacitors: a quantum capacitor (C_Q) and an electrostatic capacitor (C_Σ). The ballisticity of transistor model states that capacitors are measured in farads per meter. The three capacitors shown in Figure 4; the gate capacitor (C_G), source capacitor (C_S), and drain capacitor (C_D)—combine to form an electrostatic capacitor. A ballistic transistor circuit model is shown in this illustration. Through the three capacitors depicted, the gate, drain, and source potentials regulate the potential at the top of the barrier, or Uscf (self-consistent potential). The placement of the source and drain Fermi levels (E_{F1} & E_{F2}) and Uscf determine the mobile charge by the local density at the top of the barrier. The treatment of band filling implies the nonlinear semiconductor (or quantum) capacitance rather than clearly displaying it *(Nouri-bayat & Kashani-nia, 2017)*.

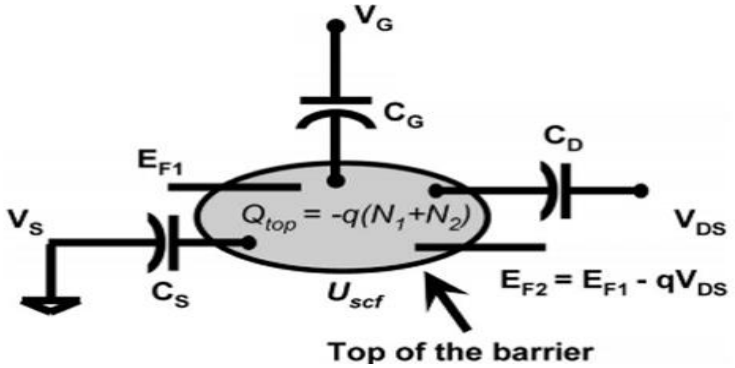

Figure 4: The Two Dimensional Circuit Model for Ballistic Transport *(Faris et al., 2022)*

Equation (9) is used to compute the gate capacitor, which is a cylindrical capacitor. The relationships between the source, drain, gate, and electrostatic capacitors in the FETToy model are shown in equation (10). The software input is given as Ag, and C_G is computed in relation to the diameter of the nanotube. Equation (10) can be used to compute the source capacitor, drain capacitor, and electrostatic capacitor. In fact, the nanotube diameter (d), insulator thickness (t), dielectric constant (ε), and effectiveness coefficient of the gate capacitor on the

electrostatic capacitor (α_G) are the inputs used by the FETToy software. The quantum capacitance is represented by equation (11), where D(E) is the local density of states, f (E− E_F) is the Fermi-function in equilibrium, and E_F is the Fermi-level *(Nouri-bayat & Kashani-nia, 2017)*.

$$C_G = 2\pi\varepsilon / \ln\left(\frac{(t+d/2)}{(d/2)}\right) \quad (9)$$

$$\propto_S = C_S/C_\Sigma, \propto_D = C_D/C_\Sigma, \alpha_G = C_G/C_\Sigma \quad (10)$$

$$C_Q = \frac{d(qN)}{d(-U_{scf}/q)} = q^2 \int_{-\infty}^{+\infty} D(E)\left(-\frac{\partial f(E-E_F)}{\partial E}\right) dE \quad (11)$$

The drain current is evaluated from

$$I_D = \int_{-\infty}^{+\infty} J(E)\,[f_1(E) - f_2(E)]dE \quad (12)$$

Where

$f_1(E) = f\left(E + U_{scf} - E_{F_1}\right)$ and

$f_2(E) = f\left(E + U_{scf} - E_{F_2}\right)$

J (E) is the "current-density-of-states.

The model is defined in terms of two densities-of-states, one for the carrier density, D(E), and one for the current density, J(E), which can be determined directly from the semiconductor bandstructure *(Rahman et al., 2002.)*.

Table 1 presents the six different dielectric materials used as gate insulators in the CNTFET structure along with their respective relative dielectric constants.

Table 1: The Six Dielectrics Used In This Research

Name of gate dielectric material	Chemical formula	Dielectric constant
Silicon dioxide	SiO_2	3.9
Aluminium oxide	Al_2O_3	9
Yttrium(III) oxide	Y_2O_3	15
Tantalum (V) oxide	Ta_2O_5	22
hafnium oxide	HfO_2	25
Lanthanum oxide	La_2O_3	30

RESULTS AND DISCUSSION

This section provides the investigation results of how temperature changes affect the performance of CNTFETs based on the use of high-k dielectric materials. The analysis focuses on the key performance indicators, including the ON current, Drain Induced Barrier Lowering (DIBL), Sub-threshold swing (SS), Transconductance, and Injection Velocity.

Variation of Temperature

The current-driven transistor devices usually have different operating temperatures due to variations in the device resistance and the characterization environment. It is thus important to determine how the environmental and experimental temperature affects the device properties of CNTFET (*Nayan et al., 2019*). This paper has explored the impact of various High-K dielectric material on the performance of CNTFET by changing the temperature 300 K to 1000 K.

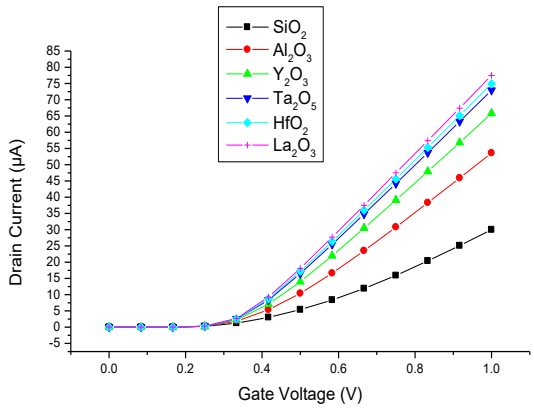

Figure 5: Temperature at 300 K

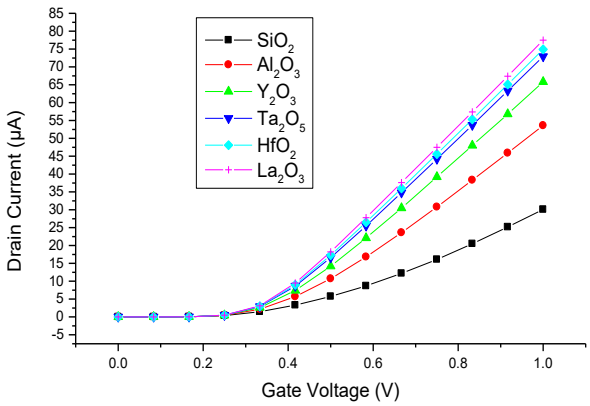

Figure 6: Temperature at 350 K

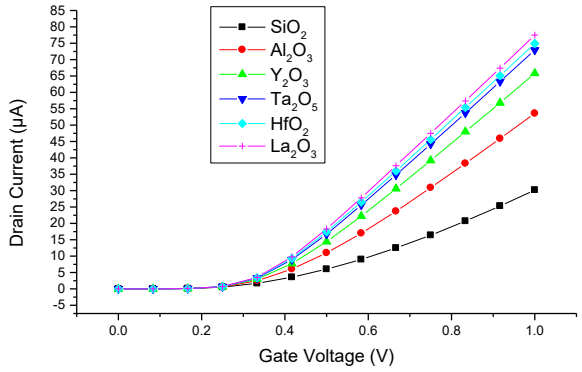

Figure 7: Temperature at 400 K

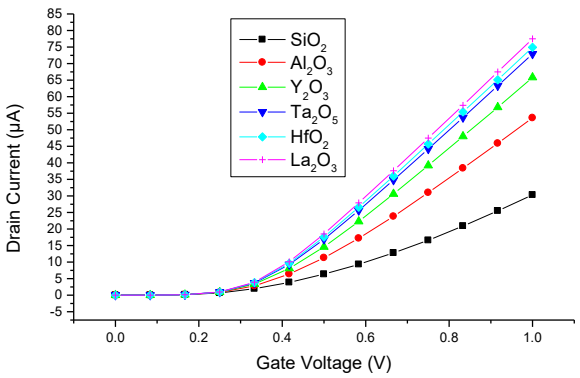

Figure 8: Temperature at 450 K

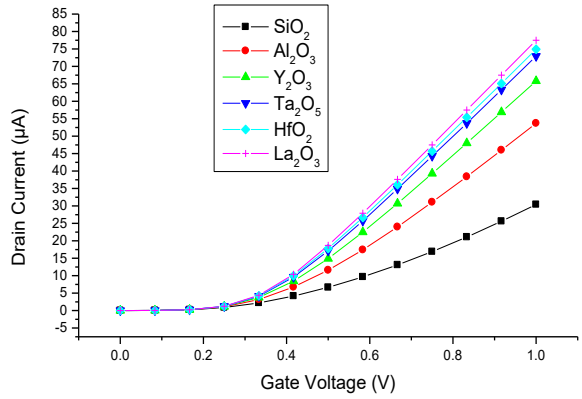

Figure 9: Temperature at 500 K

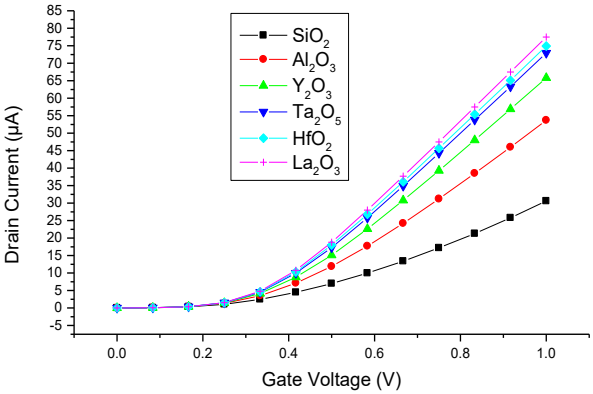

Figure 10: Temperature at 550 K

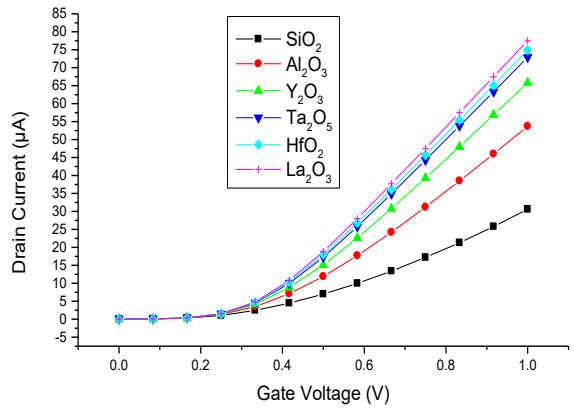

Figure 11: Temperature at 600 K

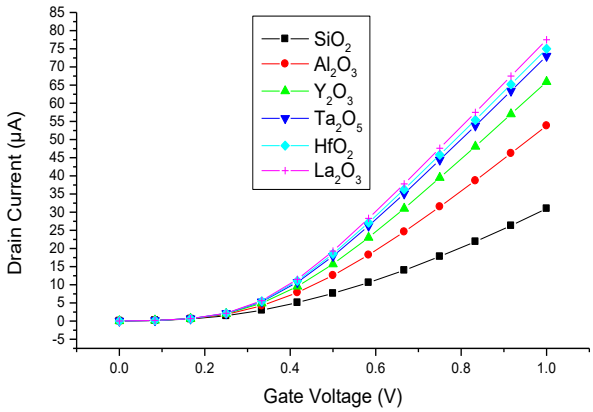

Figure 12: Temperature at 650 K

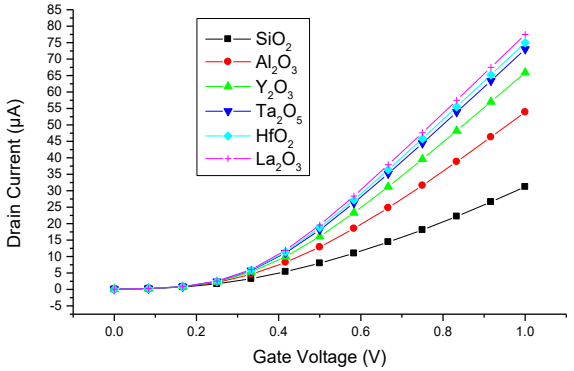

Figure 13: Temperature at 700 K

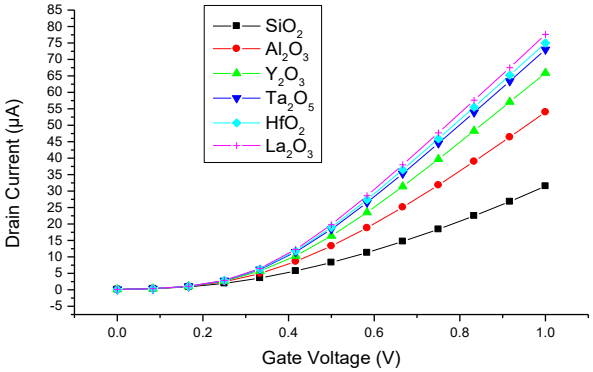

Figure 14: Temperature at 750 K

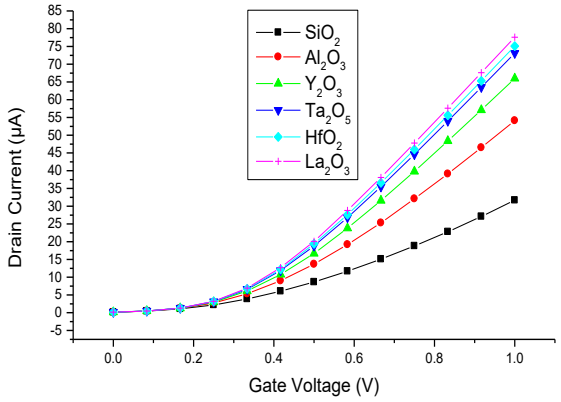

Figure 15: Temperature at 800 K

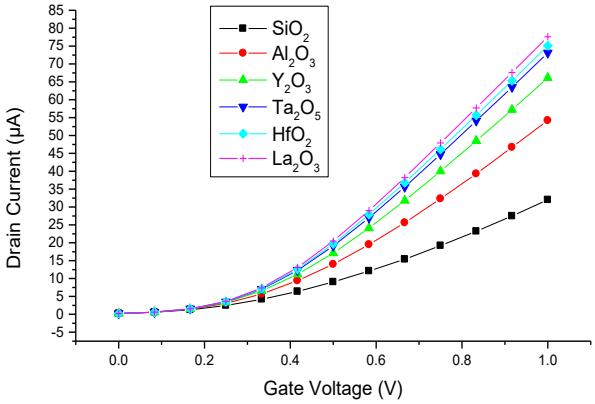

Figure 16: Temperature at 850 K

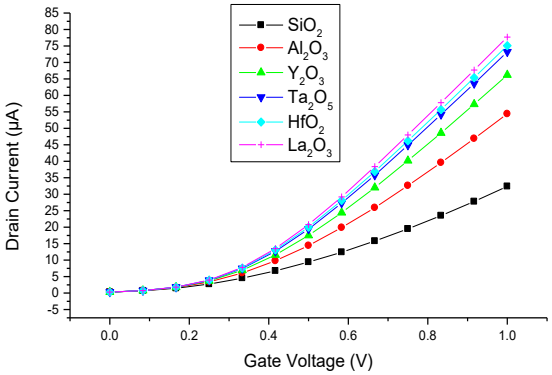

Figure 17: Temperature at 900 K

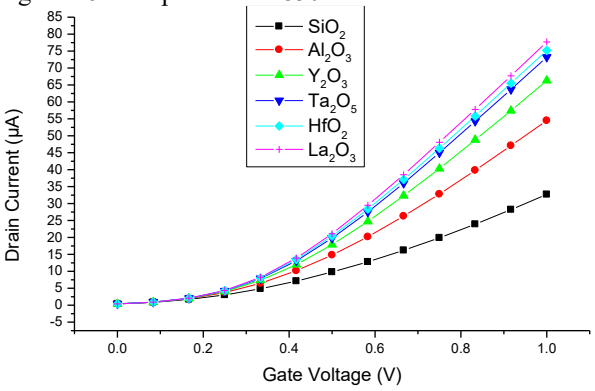

Figure 18: Temperature at 950 K

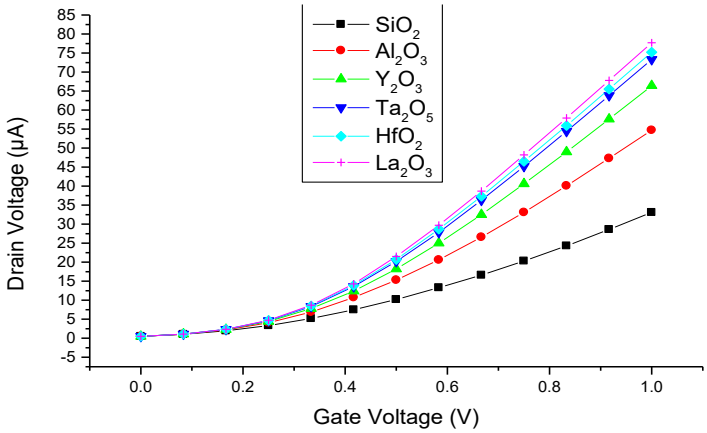

Figure 19: Temperature at 1000 K

When the drain current vs the gate voltage was plotted in each range of temperatures, it was observed that the threshold voltage of all the dielectric materials is independent of all the temperature ranges. Also, it was discovered that the drain current (I_d) increased with the gate voltage (v_g) and with the dielectric constant of the gate material in all temperature conditions. Plots at the temperatures (300 K, 350 K, 400 K, 450 K, 500 K, 550 K, 600 K, 650 K, 700 K, 750 K, 800 K, 850 K, 900 K, 950 K, & 1000 K) in Figure 5-19 shows that SiO_2, has the lowest drain current at all temperature ranges. In line with the findings of *(Nayan et al., 2019)* according to their report, "higher dielectric constant device shows maximum on-state current. This is because high dielectric constant increases the charge carrier injection in the tube channel." Significant variation in the OFF current was observed at different temperature ranges for all six dielectric materials, but at lower temperatures from 300 K to 600 K, the OFF current is almost the same. Therefore, variation of dielectric constant materials at lower temperatures has no significant effect on OFF state current.

Comparison of the Output Parameters of the Six High–K Dielectric Materials At 300 K, 600 K & 1000 K Temperature

The sub threshold regions of the device are Drain Induced Barrier Lowering (DIBL), threshold swing (SS), trans conductance (gm), output conductance (gd), voltage gain (A_V) and carrier injection velocity (V_{inj}) *(Tijjani et al., 2020)*. The output parameters of the six high-K dielectric materials ($SiO_2, Al_2O_3, Y_2O_3, Ta_2O_5, HfO_2, and\ La_2O_3$) was observed at different temperature ranges (300 K-1000 K) and have been analysed and compared at some specific temperatures which are; 300 K, 600 K and 1000 K as in table 2, 3 & 4 below

Table 2: Comparison Table of Output Parameters of the Six High–K Dielectric Materials at 300 K Temperature

Dielectric materials	S (mV/dec)	DIBL (mV/V)	gm (S/m)	gd (S/m)	A_V	V_{inj} (m/s)
SiO_2	67.70	41.14	5.938e-05	2.402e-06	24.72	4.210e+05
Al_2O_3	67.77	40.90	9.255e-05	3.700e-06	25.02	5.232e+05
Y_2O_3	67.80	31.70	1.072e-04	4.277e-06	25.08	5.612e+05
Ta_2O_5	67.80	-63.03	1.154e-04	4.599e-06	25.10	5.804e+05
HfO_2	67.80	-171	1.177e-04	4.688e-06	25.11	5.855e+05
La_2O_3	67.80	-497.50	1.206e-04	4.801e-06	25.11	5.918e+05

Table 3: Comparison of the Output Parameters of the Six High–K Dielectric Materials At 600 K

Dielectric materials	S (mV/dec)	DIBL (mV/V)	gm (S/m)	gd (S/m)	A_V	V_{inj}(m/s)
SiO_2	139.5	54.79	5.659e-05	2.304e-06	24.56	4.351e+05
Al_2O_3	137.56	54.45	9.182e-05	3.680e-06	24.95	5.267e+05
Y_2O_3	136.94	54.33	1.069e-04	4.277e-06	25.01	5.633e+05
Ta_2O_5	136.64	54.24	1.153e-04	4.614e-06	24.98	5.821e+05
HfO_2	136.56	54.20	1.176e-04	4.708e-06	24.97	5.870e+05
La_2O_3	136.46	54.12	1.205e-04	4.829e-06	24.94	5.932e+05

Table 4: Comparison of the Output Parameters of the Six High–K Dielectric Materials At 1000 K

Dielectric materials	S (mV/dec)	DIBL (mV/V)	gm (S/m)	gd (S/m)	A_V	V_{inj} (m/s)
SiO_2	263.62	106.80	5.384e-05	2.2466e-06	23.97	4.775e+05
Al_2O_3	245.32	99.12	8.928e-05	3.835e-06	23.28	5.467e+05
Y_2O_3	239.83	96.82	1.053e-04	4.723e-06	22.30	5.778e+05
Ta_2O_5	237.22	95.73	1.140e-04	5.327e-06	21.41	5.943e+05
HfO_2	236.5	95.45	1.164e-04	5.514e-06	21.11	5.987e+05
La_2O_3	235.73	95.11	1.194e-04	5.766e-06	20.70	6.042e+05

The sub threshold swing (SS) increases with temperature in all the six high-k dielectrics. Table 2 demonstrates that in the case ofSiO_2, and Al_2O_3 the effect of SS is minimal with lower value and the value is the same for $Y_2O_3, Ta_2O_5, HfO_2, and\ La_2O_3$ which is higher than that of SiO_2 & Al_2O_3 at 300 K temperature. The subthreshold swing also decreases slightly with an increase in the dielectric constant at 600 K. SS is reduced substantially at 1000 K with increasing dielectric constant; the highest values are in SiO_2 (263.62 mV/dec) and the lowest values are in La_2O_3 (235.73 mV/dec). SS tells you how fast transistor switches from OFF state to ON state (smaller value gives sharper switching).

The drain induced barrier lowering (DIBL) at 300 K from Table 2 shows that it reduces drastically as the value of dielectric material increases, higher dielectric materials (Ta_2O_5, $HfO_2, and\ La_2O_3$) shows negative value of DIBL. At 600 K temperature, DIBL shows a slight decrease as the dielectric constant materials increases. A significant decrease has been noted at 1000 K temperature in DIBL forSiO_2, Al_2O_3 & Y_2O_3, while for $Ta_2O_5, HfO_2, and\ La_2O_3$ shows a slight change in DIBL at the same temperature. DIBL is a short channel effect that causes leakage current, at all temperature ranges observed, La_2O_3 shows the least value of DIBL while SiO_2 shows the highest value at all the observed temperature ranges.

Transconductance (gm), Output conductance (gd) and carrier injection velocity (V_{inj}) all enhances with the increase in dielectric constant materials at the temperatures of 300 K, 600 K and 1000 K. Transconductance is a measure of the efficiency with which the gate controls current flow in the channel hence high transconductance provides a better gate control and La_2O_3 exhibits the highest transconductance at all temperatures at which it was observed. The overall transistor efficiency is better characterized by high carrier injection velocity, La_2O_3 also shows higher values at observed temperatures. At 300 K and 600 K temperature, La_2O_3 shows the highest values of the gain (A_V) and SiO_2

with the least values, but at high temperature of 1000 K SiO_2 shows the highest value while La_2O_3 shows the least value, the gain (A_V) describes amplification capability of a transistor.

Comparison of Output Parameters for Some High-K Dielectric Constant at Room Temperature of CNTFETs with Related Works

Table 5: Comparison of Output Parameters of Sio_2 Dielectric Constant at 300 K Temperature

Output parameters	CNTFET with SiO_2 dielectric constant from present results	CNTFET with SiO_2 dielectric constant by Tijjani et al., (2020)
Carrier injection velocity (v_{inj}) m/s	4.210 e+05	2.251 e+05
Threshold swing (SS) mV/dec	67.70	67.72
Transconductance (gm) S/m	5.938 e-05	1.609 e-05
Threshold Voltage (V_{th}) V	0.32	0.25

Table 6: Comparison of Output Parameters of Hfo_2 Dielectric Constant at 300 K Temperature

Output parameters	CNTFET with HfO_2 dielectric constant by Simulation from present results	CNTFET with HfO_2 dielectric constant by Simulation, of (Tijjani et al., 2020)	CNTFET with HfO_2 dielectric constant by Experiment findings of (Guo et al., 2004)
Carrier injection velocity (v_{inj}) m/s	5.855 e+05	3.535 e+05	3.0 e+05
Threshold swing (SS) mV/dec	67.80	67.71	70
Transconductance (gm) S/m	1.177 e-04	8.943 e-05	1.2 e-05
Threshold Voltage (V_{th}) V	0.32	0.25	≈0.35

Table 5 & 6 shows comparison of output parameters of HfO_2 dielectric constant at 300 K temperature together with that of Tijjani et al., (2020) and experimental finding of Guo et al., (2004). Some input parameters like the gate voltage and oxide thickness are not identical across the comparison. The present results were obtained at highest gate voltage of 1V and gate oxide thickness of 1.5nm thick, while that of tijjani et al (2020) was obtained at 0.6V gate voltage & 0.3nm gate oxide thickness.

From the above tables 5 & 6 it can be seen that HfO_2 which is a high-k, provides significantly higher carrier velocity and transconductance compared to SiO_2, while maintaining the same threshold voltage (Vth) and near-ideal swing (SS) in the present work which is in good agreement with that of Tijjjani et al., (2020). Therefore, high-k dielectrics allow higher gate capacitance, leading to better channel control and drive current.

CONCLUSION

This research has given an in-depth analysis of the impact of temperature variation and high-k gate dielectric on CNTFET performance. The results clearly indicate that the choice of dielectric material can play a major role in the performance of the devices. Due to enhanced gate capacitance and enhanced control of the electrostatic channel it was demonstrated that materials with higher dielectric constants significantly enhance key performance figures, including ON current, transconductance, and carrier injection velocity. Particularly, La_2O_3 remained superior to the rest of the dielectric materials considered in this study. Conversely, it was found out that changes in temperature adversely affected the performance of devices. Another remarkable increase in OFF current and subthreshold swing was observed as the temperature was increased 300 K to 1000 K, which presents a decrease in switching efficiency. Moreover, with increased temperatures, short-channel effects such as the drain-induced reduction of the barrier were more pronounced, which could negatively affect power consumption and the reliability of a device. Another fundamental trade-off between the performance loss due to thermal effects and the increased electrostatic control offered by the high-k dielectric is also noted in the findings. Consequently, though high-k materials enhance CNTFET performance at low temperatures, their effectiveness is not that effective when operating at high temperatures. In conclusion, high-k gate dielectrics of CNTFETs are a promising path to more scaled and efficient nanoelectronic devices in the future. Nevertheless, both thermal effects and material characteristics should be taken into account to ensure the most efficient work of the device. Future studies can focus on advanced device architecture, improved thermal management solutions, and combined integration of materials to improve the performance of CNTFET further.

REFERENCES

Agarwal, A., Lang. J. H. (2005). Foundations of Analog and Digital Electronic Circuits". Morgan Kaufmann

publishers, 500 Sansome Street, San Francisco, CA 94111 ISBN: 1-55860-735-8

Appenzeller, J., Knoch, J., Martel, R., Derycke, V., Wind, S. J., Member, S., & Avouris, P. (2002). Carbon Nanotube Electronics. IEEE Transactions on Nanotechnology, vol. 1, no. 4, 184–189.

Buchanan, A. (1999). Scaling the gate dielectric: Materials, integration, and reliability. IBM J. Res. develop. vol. 43 no. 3

Dass, D., Prasher, R., & Vaid, R. (2013). Impact of Scaling Gate Insulator Thickness on the Performance of Carbon Nanotube Field Effect Transistors (CNTFETs). Journal of NANO- and electronic physics vol.5 (2), 02014(6pp) 1–6.

Demkov, A. A., & Navrotsky, A. (2005). Materials Fundamentals of Gate Dielectrics. Springer, P.O Box 17, 3300AA Dordrecht, the Netherlands ISBN-13 978-1-4020

Dixit, A., & Gupta, N. (2020). Simulations of the CNFETs using different high- k gate dielectrics. Bulletin of Electrical Engineering and Informatics Vol. 9, No. ISSN: 2302-9285, 9(3), pp. 943–949. https://doi.org/10.11591/eei.v9i3.1784

Faris, M., Hadi, A., Mara, U. T., Mara, U. T., Mara, U. T., & Wahab, Y. A. (2022). Effects of Different Oxide Thicknesses on the Characteristics of CNTFET. IEEE Regional Symposium on Micro and Nanoelectronics (RSM) 58–61.

Guo, J., Member, S., Datta, S., & Lundstrom, M. (2004). A Numerical Study of Scaling Issues for Schottky-Barrier Carbon Nanotube Transistors. IEEE Transactions of electron devices Vol 51, No. 2, 172–177.

Hegde, V. N., Manju, V. V, & Hemaraju, B. C. (2024). Frequency and temperature dependent dielectric properties of CuO nanoparticles. Chemical Physics Impact, 8(3), 100474. https://doi.org/10.1016/j.chphi.2024.100474

Hierold, C. (2008) "Advanced Micro & Nano Systems". WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim ISBN: 978-3-527--31720-2 (Vol. 8).

Hornyak, G. L., Moore, J. J., Tibbals, H. F., & Dutta, J. (2009). "Fundamentals of Nanotechnology". CRC Press Taylor & Francis Group Boca Raton London Newyork

Hossain, S. R., Sultana, S., Rahman, A., & Imam, S. (2025). Temperature and Dielectric Constant Dependent Input and Output Characteristics of CNTFET. Micro&NanoLetters, John Wiley & Sons Ltd1–10. https://doi.org/10.1049/mna2.70010

Javey, A., Qi, P., Wang, Q., & Dai, H. (2004). Ten- to 50-nm-long quasi-ballistic carbon nanotube devices obtained without complex lithography. The National Academy of Sciences of the USA (Track II), 4–6 www.pnas.org/cgi/doi/10.1073/pnas.0404450101.

Kim, Y. (2010). Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics. 11(3), 93–105. https://doi.org/10.4313/TEEM.2010.11.3.093

Kumari, A., Rani, S., & Singh, B. (2019). Parameterized Comparison of Nanotransistors Based on CNT and GNR Materials : Effect of Variation in Gate Oxide Thickness and Dielectric Constant. Journal of ELECTRONIC MATERIALS https://doi.org/10.1007/s11664-019-07062-4.

Naderi, A., Noorbakhsh, S. M., & Elahipanah, H. (2012). Temperature Dependence of Electrical Characteristics of Carbon Nanotube Field-Effect Transistors : A Quantum Simulation Study. Hindawi Publishing Corporation Journal of Nanomaterials Volume 2012, Article ID 532625, 7 pages https://doi.org/10.1155/2012/532625

Nayan, F., Tahsin, S., & Chowdhury, N. (2019). Performance Analysis of Nanoscale Carbon Nanotube Field Effect Transistor considering the Impacts of Temperature and Gate Dielectrics. International Conference on Advances in Electrical Engineering (ICAEE), 26–28.

Nouailhat, A. (2008). An Introduction to Nanoscience and Nanotechnology. ISTE and John Wiley & sons, Inc, Britain and United States.

Nouri-bayat, R., & Kashani-nia, A. R. (2017). Designing a Carbon Nanotube Field-Effect Transistor with High Transition Frequency for Ultra-Wideband Application. Scientific Research Publishing Inc. Engineering, 9, 22–35. https://doi.org/10.4236/eng.2017.91003

Park, J., Rosenblatt, S., Yaish, Y., Sazonova, V., Hande, U., Braig, S., Arias, T. A., Brouwer, P. W., & Mceuen, P. L. (2004). Electron − Phonon Scattering in Metallic Single-Walled Carbon Nanotubes. NANO LETTERS Vol. 4, No. 3 517-520, 10.1021/nl035258c

Rahman, A., Guo, J., Datta, S., Lundstrom, M., & Lafayette, W. (2002). Invited Paper Theory of Ballistic Nanotransistors. 3515, 1–38.

Saleh, H. M., & Koller, M. (1991). Carbon Nanotubes. 1–7. DOI: http://dx.doi.org/10.5772/intechopen.85387

Sinha, S. K., & Chaudhury, S. (2012). Oxide thickness effect on quantum capacitance in single-gate MOSFET and CNTFET devices. 2012 Annual IEEE India Conference, INDICON 2012, 42–46. https://doi.org/10.1109/INDCON.2012.6420586

Talin, A. A. (2018). Carrier transport mechanisms in semiconductor nanostructures and devices. Journal of Semiconductors, Vol. 39, No. 6, https://doi.org/10.1088/1674-4926/39/6/061002

Tijjani, A., Galadanci, G. S. M., & Babaji, G. (2020). Drain Current Characteristics of Carbon-nanotube FET (CNTFET) with Sio2, Zro2 and Hf02 as Dielectric Materials using FETToy Code. NIPES - Journal of Science and Technology Research, 2(2), 212–227. https://doi.org/10.37933/nipes/2.2.2020.22

Tijjani, A., Galadanci, G. S. M., Babaji, G., Gana, S. M., & Galadima, B. Y. (2022). Temperature variation effects on Carbon Nanotube Field Effect Transistor (CNTFET) based on simulation study. Bayero Journal of Pure and Applied Sciences, 13(1), 204–210. http://dx.doi.org/10.4314/bajopas.v13i1.33S

Xing, W. Yin, S. Member, L. Liu, and J. Huang. (2011). Investigation on Self-Heating Effect in Carbon. IEEE Transactions on Electron Devices, 58(2), 523–529., vol. 58,

Yacobi, B. G. (2004). Semiconductor Materials. B. G. Kluwer Academic/Plenum Publishers, New york, Boston, Dordrecht London, Moscow. eBook ISBN: 0-306-47942-7 Print ISBN: 0-306-47361-5