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Evaluation of the Influence of Gate Dielectric Materials on the Temperature Sensitivity of Silicon Nanowire Transistors

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ABSTRACT

Nanowire-based sensors face a persistent bottleneck: improving electrostatic control via high-κ dielectrics often compromises their thermal responsiveness. To resolve this tension, we investigated the temperature-dependent drain current (250 K–450 K) of silicon nanowire transistors employing four distinct gate dielectrics: SiO_2 (silicon dioxide), Al_2O_3 (aluminum oxide), ZrO_2 (zirconium oxide), and HfO_2 (hafnium oxide). Our analysis reveals that the temperature sensitivity is inversely proportional to the dielectric constant (κ). Although HfO_2 (κ=25) provides the strongest gate control and maximum drive current, its superior electrostatic screening actually suppresses the channel's intrinsic thermal carrier-generation effect, resulting in minimal sensitivity. In stark contrast, SiO_2 (κ=3.9) allows the temperature-dependent carrier density to dominate transport, yielding the highest sensitivity, approximately 9×10^{-7} A/m/K. We conclude that dielectric engineering is not a one-size-fits-all proposition; rather, the choice of dielectric must be dictated by whether the target application prioritizes drive-current density (HfO_2) or thermal detectivity (SiO_2).

Keywords:
Dielectric materials,
Electrostatic control,
Temperature sensitivity,
Transconductance,
Nanowire transistors.

INTRODUCTION

As Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) approach their scaling limits, there was a significant shift in nanoscale research towards finding the architecture that can play a role in sustaining the continued device downscaling which could eventually minimize the short channel effects (SCEs) (Chopade & Padole, 2017; Minhaj et al., 2019; Vimala et al., 2019; Das et al., 2023). One of these architectures is the Nanowire Field Effect Transistor (NWFET). Silicon nanowire field effect transistors (Si-NWFETs) have emerged as potential candidates for Moore's Law extension beyond sub-20 nm technology node owing to their superior electrostatic control and minimized SCEs (Sacchetto et al., 2008; AlAriqi et al., 2019; Li et al., 2021). In recent years, Si-NWFETs have garnered significant scholarly interest because of their capability to provide enhanced channel control. These advantages make them appropriate for low-power electronics, integrated circuits and nanoscale sensing applications. Nanowire transistors have specifically demonstrated significant prospective as temperature sensitive devices due to their strong dependence of electrical properties on thermal variations. It is therefore significant to understand the influence of temperature on nanoelectronic device for the design and optimization of reliable electronic systems and high-performance nanosensors. The gate dielectric material plays a pivotal role in determining carrier transport, electrostatic coupling, leakage current, threshold voltage stability and the sensitivity of nanoelectronic device. Silicon dioxide (SiO_2) being the conventional dielectric material has long been used as the standard gate dielectric material owing to its excellent interface quality with silicon. However, continued device scaling has driven the introduction of high dielectric constant materials such as aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), and hafnium oxide (HfO_2). These materials provide improved gate capacitance requiring very thin layers leading to enhanced gate control and reduced leakage current.

Several studies have explored the electrical performance of nanowire field effect transistors utilizing different high-k dielectric materials and the temperature sensitivity of nanowire transistors. Kosmani et al. (2020) demonstrated that the use of high-k materials enhances gate control and electrical performance of nanowire transistors. For biosensor applications, Popov et al. (2022) fabricated parallel nanowire SOI (silicon-on-insulator) transistors with a high-k HfO_2/AL_2O_3 gate oxide stack, illustrating enhanced device stability in liquid

environments and improved sensitivity through the use of high-k dielectrics. Thakur and Chaturvedi (2021) demonstrated that HfO_2-based nanowire transistors attain significant performance improvement with a 122 μA increase in drive current and a current ratio of 10^7, which made them suitable for digital applications. Temperature-dependent studies exhibit that subthreshold swing and DIBL (drain-induced barrier lowering) increase linearly with the increase in temperature while current ratio increases exponentially in Si-NWTs (Hashim & Sidek, 2011). Agha et al. (2021) examined the effect of operating temperature on a gate-all-around silicon nanowire TFET and found that lower temperatures improve its electrical performance, highlighting its potential for temperature sensing applications. For temperature sensing applications, optimal sensitivity is attained with 5 nm oxide thickness and channel lengths between 25-85 nm (Li et al., 2021; Das et al., 2023). Prates et al. (2024) conducted a comprehensive experimental comparison of junctionless (JL) and inversion-mode (IM) nanowire MOSFETs fabricated with identical gate stacks and state-of-the-art processes across a temperature range of 300–580 K. Their evaluation revealed that IM nanowire transistors exhibit superior electrical performance, demonstrating three times higher maximum transconductance, three times higher conduction current, and twice the low-field mobility compared to JL counterparts with a 10 nm fin width at a given temperature. Thakur et al. (2025) investigated the temperature-dependent performance of a GaSb/Si/SiGe heterojunction vertical nanowire (V-NW) junctionless field-effect transistor (JLFET) designed for logic circuit applications. Their simulation study across 300–500 K revealed that the GaSb source increases the source-channel barrier height, effectively mitigating short-channel effects even at elevated temperatures. Verma and Saket (2026) investigated the temperature-dependent performance of silicon (Si), germanium (Ge), and gallium arsenide (GaAs) nanowire field-effect transistors (NWFETs) using atomistic quantum transport simulations across a temperature range of 223–473 K. Their findings revealed that increasing temperature universally degrades the subthreshold slope and elevates leakage current due to thermally generated carriers, with Ge-NWFETs (Germanium-nanowire field effect transistors) exhibiting the highest current drive but pronounced temperature sensitivity. Kaur et al. (2026) examined the temperature-dependent performance of a dual-material gate SiGe/Si (Silicon-Germanium/Silicon) nanowire field effect transistors for sensing applications. Their results showed improved temperature stability, reduced leakage current and power consumption, and enhanced linearity, demonstrating the device's suitability for reliable temperature sensing.

However, little attention has been dedicated to understanding how dielectric engineering affects temperature sensitivity and performance of nanowire transistors.

Temperature sensitivity is a critical figure of merit for nanowire-based sensing applications because it determines the capability of a nanowire transistor to respond to ambient temperature variations. The gate dielectric constant has a direct influence on device channel electrostatics and carrier transport mechanisms as a result of which the magnitude of temperature-induced current gets affected. Thus, a systematic examination of the relationship between gate dielectric material and temperature sensitivity is required to identify appropriate candidates for advanced nano-sensing applications.

In this work, the impact of four gate dielectric materials namely, (SiO_2), (Al_2O_3), (ZrO_2) and (HfO_2), on the temperature sensitivity of nanowire transistors was evaluated using the PADRE(Poisson And DRift-diffusion Equations) simulator in the MuGFET (Multigate Field Effect Transistor) tool simulation environment. The electrical properties of the devices were analyzed over a temperature of 250 K to 450 K. The crucial performance parameters investigated include drain current, transconductance, transfer characteristics and temperature sensitivity to determine the influence of dielectric materials on thermal response of the devices. The findings provide worthwhile insights into dielectric engineering strategies for optimizing silicon nanowire transistors for nano-sensing applications.

Device Structure

Figure 1 shows the Si-NWFET's (Silicon nanowire field effect transistor's) device architecture. The source, drain, gate, and gate oxide are some of its crucial components. The source and drain represent the charge injection and collecting regions, respectively, and the gate is the control terminal that alters the carrier flow across the nanowire channel. When positioned between the gate electrode and the channel, the gate oxide provides the necessary insulation and enables effective electrostatic control over the channel. Together, these components define the Si-NWFET's operating characteristics and are crucial for defining its performance and short-channel behavior.

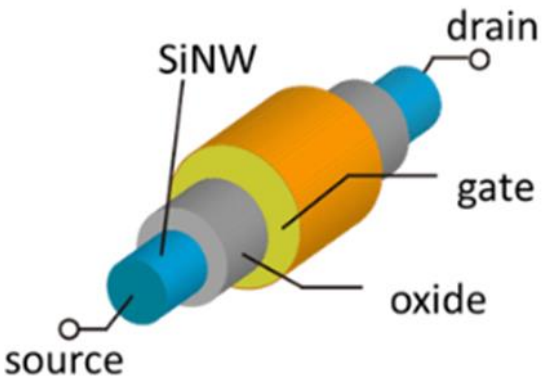

Figure 1: Si-NWFET Device Structure (Khan et al., 2015)

Theoretical Background

The temperature sensitivity of silicon nanowire transistors (Si-NWFETs) is governed by the interplay between electrostatic control and charge carrier transport, temperature-dependent properties of semiconductor materials, all of which are influenced by the gate dielectric material. To describe these physical mechanisms and the influence of different gate dielectrics on the nanowire temperature sensitivity, this work employed the Poisson equation, the drift-diffusion equation, the temperature-dependent drain current and temperature sensitivity relationships. These governing equations provide the theoretical foundation for interpreting the simulation results presented in this work. Specifically, Equation (1) describes the temperature-dependent mobility degradation that underpins the trans conductance behavior discussed in Section 4.3. Equation (3) establishes the relationship between temperature and drain current, which is used to extract the sensitivity coefficient S_T defined in Equation (4). The observed inverse scaling between dielectric constant (k) and temperature sensitivity (Section 4.2), can be understood through these equations: high-k dielectrics increaseC_{ox}, thereby improving electrostatic control and suppressing the influence of temperature-dependent mobility fluctuations on drain current.

Mobility–Temperature Relationship equation describes the influence of temperature on carrier mobility (Most Fundamental) is given by (Singh et al., 2006; Auth et al., 2012):

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{-M} \quad (1)$$

Where $\mu(T)$ is the carrier mobility at operating temperature T. It indicates how easily electrons or holes move through the nanowire channel, μ_0 is the carrier mobility at reference temperature (T_0) usually 300 K, T is the operating temperature of the transistor (K), T_0 is the reference temperature typically 300K, and M is the mobility degradation coefficient (≈1.5–2.5) (Kuhn, 2012).

The Drain Current Relationship of a nanowire transistor with temperature can be obtained using the Drain Current Relationship given by (Kuhn, 2012):

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (2)$$

Where I_D is the drain current flowing through the transistors, μ is the carrier mobility, C_{ox} is the oxide capacitance per unit area, W is the channel width, L is the channel length of the transistor, V_{GS} is the gate-to-source voltage and V_{th} is the threshold voltage.

Substituting equation 1 in equation 2, gives the new equation which combines the channel length temperature, mobility degradation, and the drain current. The new equation is given by:

$$I_D(T) = \frac{\mu_0 C_{ox}}{2} \left(\frac{T}{T_0}\right)^{-m} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (3)$$

Where $I_D(T)$ is the temperature-dependent drain current. Temperature sensitivity coefficient (S_T) expresses how much each electrical parameter changes with temperature. A larger absolute value of S_T means the device parameter changes more for a given temperature change. In recently published works related to silicon nanowire transistors, the normalized temperature sensitivity coefficient was widely used, since the values can be compared across various device parameter changes due to temperature changes. It can be expressed as (Colinge et al, 2010):

$$S_T = \frac{1}{P} \frac{dP}{dT} \quad (4)$$

Where S_T is the temperature sensitivity coefficient, P electrical parameter under investigation (such as threshold voltage, drain current, subthreshold swing, and the leakage current), $\frac{dP}{dT}$ is the rate of change of the electrical parameters with temperature. This coefficient allows comparison of different channel lengths and different nanowire materials.

MATERIALS AND METHODS

In this research a simulation software called PADRE (Poisson and DRift-diffusion Equations) was used throughout the work. It is one of the important components in MuGFET (Multigate Field Effect

Transistor) tool which is available on nanohub.org. The software consistently solves the Poisson and drift-diffusion equations which ensures reliability in the device modelling (Bhat et al., 2015). This simulator is well suited for generating useful current-voltage characteristics that paves the way for understanding the fundamental physics of FETs. In this study, four different gate dielectrics namely, Silicon Dioxide (3.9), Aluminum Oxide (9), Zirconium Oxide (22) and Hafnium Oxide (25), across a temperature range of 250 K to 450 K was investigated while keeping the gate length fixed at 20 nm and the oxide thickness at 2 nm. The channel doping concentration was maintained at 1×10^{16} cm^{-3}, with source and drain doping concentrations of 1×10^{19} cm^{-3}. The applied bias conditions included a drain voltage sweep from 0.05 V to 1 V and a gate voltage sweep from 0 V to 1 V. To investigate the temperature sensitivity of the device, the temperature was varied over the specified range, and the corresponding changes in the drain current, transconductance and dielectric constants for the different dielectric materials were analyzed.

RESULTS AND DISCUSSION

Results of a simulation showing the influence of different gate dielectrics (silicon dioxide, aluminum oxide, zirconium oxide, and hafnium oxide) on temperature sensitivity in silicon nanowire field effect transistors are discussed in this section.

Effect of Temperature on Drain Current

The variation of drain current with respect to the temperature of silicon nanowire transistors for different dielectric materials is shown in Figure 2, in which silicon dioxide, aluminum oxide, zirconium oxide, and hafnium oxide are used as gate dielectric materials. It was observed that the drain current increases as temperature increases for all the dielectric materials. At higher temperatures, the carrier mobility increases due to greater carriers (Kim et al., 2020), and their higher kinetic energy, which enables them to traverse the channel more easily. The nanowire transistor device with HfO_2 shows a higher drain current of 0.0027 A/μm around 450K because high-k dielectrics provide superior electrostatic coupling between the gate and the channel. Our findings agree with the work of Kosmani et al (2020) and Thakur and Chaturvedi (2021) that high-k gate materials enhance gate control and electrical performance of nanowire transistors. Consequently, the use of high-k dielectrics contributes to improved performance of the transistor in terms of current drive capability.

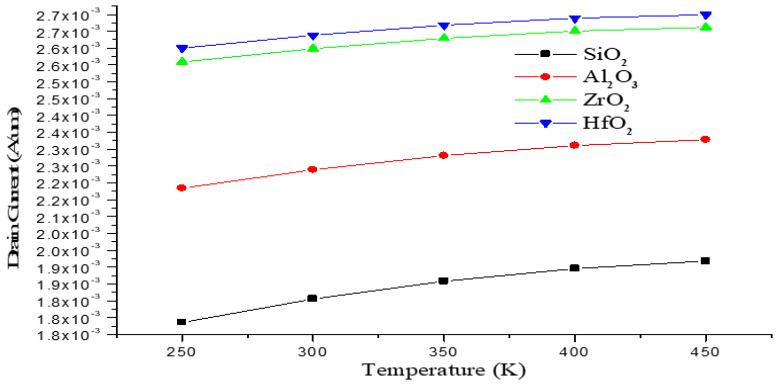

Figure 2: Drain current (I_D) as a function of temperature for si-NWFETs with four different dielectric materials (SiO_2, Al_2O_3, ZrO_2, and HfO_2)

Effect of Temperature on Dielectric Constant

The influence of the dielectric constant on temperature sensitivity of the transistor is plotted in Figure 3, which depicts the temperature sensitivity versus the dielectric constant of various gate dielectric materials, including SiO_2, Al_2O_3, ZrO_2, and HfO_2. From the graph, it was observed in Figure 3 that the sensitivity decreases as the dielectric constant of gate dielectric materials increases. These results indicate that Si nanowire transistors with high-k dielectrics have low temperature sensitivity due to their better channel electrostatic control. The dielectric constant of 3.9 (which corresponds to SiO_2) has the highest temperature sensitivity of about 9×10^{-7} A/m/K compared to the others.

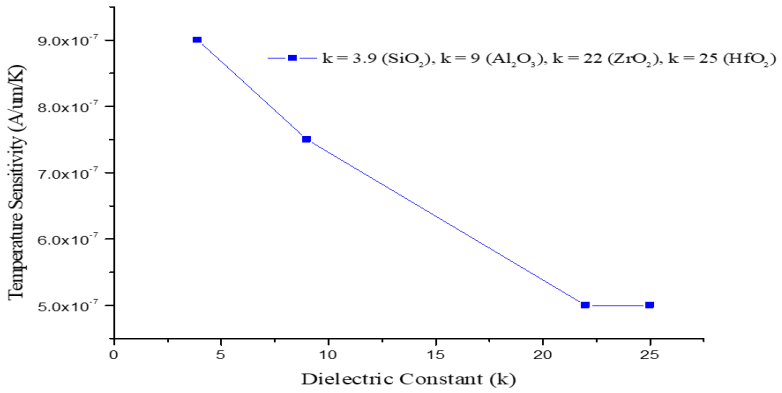

Figure 3: Temperature sensitivity as a function of dielectric constant (k), showing the inverse relationship between k and thermal sensitivity

Effect of Temperature on Transconductance

Figure 4 shows how transconductance varies with different temperatures for devices of silicon dioxide, aluminum oxide, zirconium oxide, hafnium oxide, etc. as gate dielectric materials. The transconductance varies inversely with the temperature for all dielectrics studied. The temperature dependence is mainly due to phonon scattering increasing at high temperatures, which results in a decrease in channel mobility, and, therefore, the transconductance decreases as the temperature increases (Pérez-Tomás et al., 2012). Also from Figure 4, it was observed that, among these four dielectric materials, the nanowire devices with hafnium oxide have the highest transconductance value of 0.00454 S/m at 250 K. Therefore, high-k materials will positively contribute to the improvement of transconductance for nanowire transistors, even with temperature-dependent effects (Kim et al., 2020). Our findings are consistent with and extend the observation of several prior studies such as Das et al (2023) that demonstrated that HfO_2-based nanowire transistors exhibit reduced mobility and transconductance when considering the combined effects of scattering and temperature confirming that high-k dielectrics, while improving electrostatic control, may not necessarily optimize thermal performance.

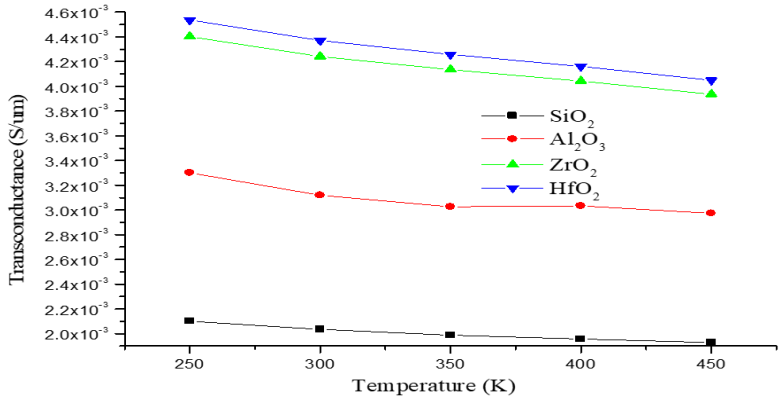

Figure 4: Transconductance as a function of temperature for si-NWFETs with four different gate dielectric materials

Transfer Characteristics

Figures 5(a-d) display the transfer characteristics of the nanowire transistors. Figure 5(a) shows how drain current changes as a function of gate voltage at different temperatures (250 K, 300 K, 350 K, and 450 K) in a device with silicon dioxide dielectric. Figures 5(b-c) present similar plots for aluminum oxide, zirconium oxide, and hafnium oxide-based nanowire transistors, respectively. In the case of each dielectric material, the drain current increases with the increase in the gate voltage at every considered temperature. With increasing temperature, the drain current increases due to enhanced

charge carrier generation and an increase in the average energy of charge carriers in the channel (Silva et al., 2025). The results demonstrate that the devices exhibit normal transistor characteristics throughout the entire operating temperature range. Thus, we conclude that the device transfer characteristics are sensitive to the gate dielectric material. The result thus indicates the crucial role of dielectric engineering in achieving the desired performance and thermal robustness of nanowire transistors.

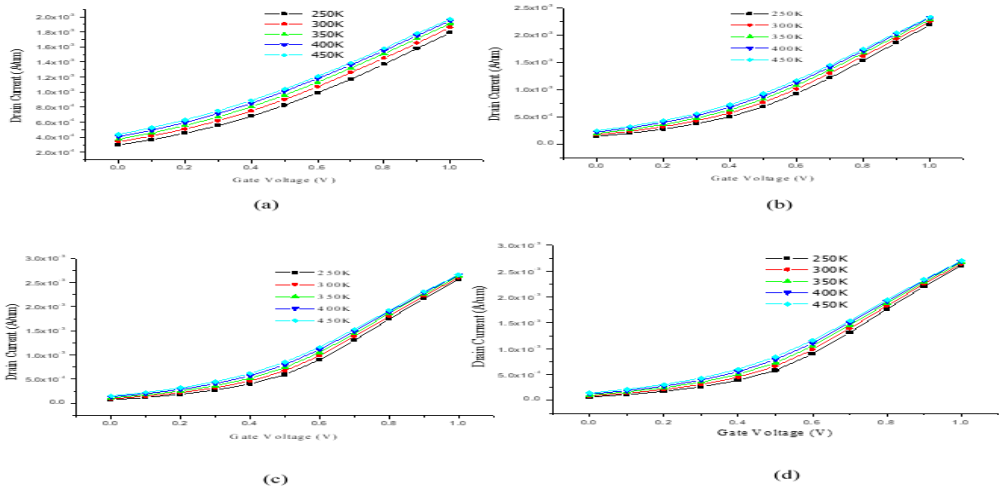

Figure 5: Transfer characteristics (I_D vs V_{GS}) of Si-NWFETs with (a) SiO_2, (b) Al_2O_3, (c) ZrO_2, and (d) HfO_2 gate dielectrics at temperatures ranging from 250 K to 450 K

CONCLUSION

This work established a quantitative, physically grounded design rule for dielectric engineering in silicon nanowire transistors: temperature sensitivity and electrostatic performance are fundamentally antagonistic, governed by the dielectric constant (κ). High-κ HfO_2 enforces rigid gate control that suppresses thermal carrier-density fluctuations, yielding superior transconductance (0.0045 S/m) but minimal thermal responsivity. Conversely, low-κ SiO_2 permits carrier-density dynamics to dominate transport, delivering maximum sensitivity (~9×10^{-7} A/m/K) at the cost of reduced drive current. Most importantly, we have shown that no single dielectric optimizes both figures of merit; instead, the best candidate is entirely determined by the target application, the stable logic and memory applications favoring HfO_2 and the thermal-sensing IoT and biomedical diagnostic applications preferring SiO_2. The observed inversely related dielectric constants and the FET sensitivities offer a prediction guideline, which is general enough for other nanostructure-based FET devices without the need for comprehensive empirical exploration of different dielectrics. Future work is expected to include the investigation of the dielectric sensitivity framework to the 2D materials-based field-effect devices to observe whether the low-k/high-k tradeoff is exaggerated or suppressed in atomically thin devices. Such a study could establish a unified design paradigm for thermal sensing across all nanoscale FET architectures.

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