Nigerian Journal of Applied Physics (NJAP)
ISSN Print: 3115-5871
ISSN Online: 3115-588X
DOI: https://doi.org/10.62292/njap-v2i3-2026-87
Volume 2(3), September 2026

Systematic Evaluation of the effect of Temperature Sensitivity and Channel Length Scaling on Electrical Performance of Nanowire Transistors

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ABSTRACT

This paper presents a comparison of the electrical performance and temperature sensitivity of Silicon Nanowire Field-effect Transistors (Si-NWFETs), Germanium Nanowire Field-effect Transistors (Ge-NWFETs), and Gallium Arsenide Nanowire Field-effect Transistors (GaAs-NWFETs) when the channel length is scaled down. To analyze the electrical behavior of the devices, the MuGFET simulator was used during the simulations and the devices were simulated at various channel lengths: 25 nm, 45 nm, 65 nm, 85 nm, and 105 nm and temperature range 250 K–450 K. The electrical properties investigated include drain current (I_D), drain induced barrier lowering (DIBL) sub threshold-swing (SS), and threshold voltage (V_{TH}). The results show that in terms of the electrical characteristics, GaAs-NWFET exhibits the lowest DIBL value of 16.68mV/V at the channel length of 105 nm, threshold voltage of 0.32 V at channel length of 25 nm; making it a nanodevice with minimized short channel effects among the three investigated devices. For temperature sensitivity, the GaAs-NWFET exhibits the overall highest drain current of 1.70 × 10^{-3}A/µm at 450 K and the channel length of 85 nm; making it the best temperature nanosensor among the three investigated nanowire transistors. The finding suggests the consideration of channel material selection and channel length optimization for designing temperature-sensitive nanodevices with reduced short channel effects.

Keywords:
Channel Length,
Electrical Characteristics,
Si-NWFTs,
Ge-NWFT,
GaAs-NWFT
Si-NWFTs,
Temperature Sensitivity.

INTRODUCTION

As semiconductor technology has advanced, the size of transistors has been shrunk to nanometer dimensions to increase speed, decrease power consumption, and increase device density. The traditional planar MOSFETs are approaching their physical limits, and new device structures like nanowire field-effect transistors (NWFETs) have been developed. These devices offer improved electrostatic control of the channel which greatly minimize short channel effects (Guerfi & Larrieu, 2016),(Pu et al., 2026),(Srivastava et al., 2025),(Kim et al., 2020),(Vimala et al., 2019). The device performance is highly sensitive to the scaling effects when the length of the channel is scaled-down below 100 nm. Some of the parameters that are affected by channel length reduction include subthreshold swing, drain current and threshold voltage, and hence tamper with the performance of nanodevices (Huang, 2022),(Al-jawadi et al., 2025). On the other hand, temperature is critical to the operation of semiconductors; higher temperature increases carrier concentration and phonon scattering, but reduces mobility, which eventually degrades device performance (Zhao et al., 2023),(Navaneetha & Bikshalu, 2023). The choice of semiconductor channel material such as silicon, germanium and gallium arsenide also plays a role towards the behavior of nanodevices. Silicon (Si) is still widely used due to its stability and advanced fabrication process. Germanium (Ge) offers higher carrier mobility and Gallium Arsenide (GaAs) has better electron transport properties(Liang et al., 2007),(Musa et al., 2025). Therefore, it is important to study the relationship between channel length scaling and temperature effects on these materials for the design of high-performance nanowire transistors.

In recent times, several researches have examined the performance of nanowire transistors at different temperatures. As the temperature increases, the leakage current increases, sub-threshold swing reduce because of thermal carrier generation (Chang et al., 2019). The threshold voltage and carrier mobility are also strongly influenced by temperature, particularly in nanoscale devices (Zhao et al., 2023). The material comparison

studies indicate that the Ge-based nanowire transistors have higher drive current because of their higher carrier mobility, but are more sensitive to temperature changes (Liang et al., 2007). On the other hand, GaAs nanowire transistors possess better electron transport and less scattering, making them suitable for high-frequency and high-temperature applications (Musa et al., 2025). Silicon devices on the other hand, offer a balanced performance with improved thermal stability and reduced leakage current (Al-jawadi et al., 2025),(Navaneetha & Bikshalu, 2023). However, most of them either focus on the effects of temperature or scaling or have little research on both aspects for multiple materials in nanowire transistors

When the nanowire-FET channel length is scaled down to very short lengths, short-channel effects such as increased leakage current and unreliable threshold voltage affect their performance. Moreover, the variation of temperature affects the device behavior by reducing the carrier mobility which in turn affects the electrical characteristics of the nanowire-FETs.(Bikshalu, & Navaneetha 2023) (Zhao et al., 2023), The effects of the scaling and temperature are different for different transistors, such as gallium arsenide nanowire FET, (GaAs-NWFET), germanium (Ge) and silicon (Si), but they are usually studied separately (Liang et al., 2007). This leads to a missing link in understanding the combined effects of channel length scaling and temperature to the electrical performance of such materials. Therefore, it is necessary to perform a combined and comparative study to know how these factors would work in conjunction and to find out the most appropriate material and channel length for stable and high-performance nanowire transistors.

The aim of this work is to systematically evaluate the effect of temperature sensitivity and channel length scaling on electrical performance of Nanowire Transistors such as silicon (Si), germanium (Ge), and gallium arsenide (GaAs) nanowire transistors.

Device Structure

The Si-NWFETs device architecture is shown in Figure 1. The device contains source, drain, gate and gate oxide. The source and the drain are the regions where charges are injected and collected, respectively, and the gate is the control terminal which modifies the flow of charge in the nanowire channel. The gate oxide, if placed between the gate electrode and the channel, will insulate the channel and can be used to control the channel with electrostatic force. These elements determine the Si-NWFETs operating characteristics and are important for the performance and short channel behavior.

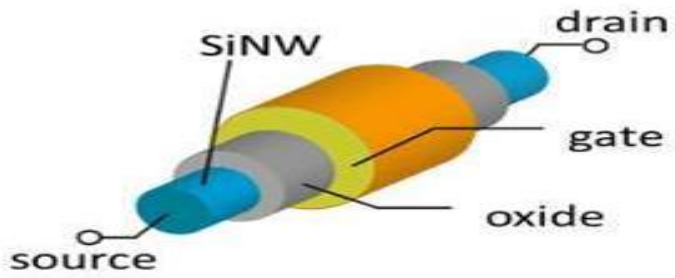

Figure 1: Si-NWFET Device Structure(Khan et al., 2015)

MATERIALS AND METHODS

Simulation Setup

In this research, we used PADRE (**P**oisson **and DR**ift-diffusion **E**quations) Simulator which is an important component of the Multigate Field Effect Transistors (MuGFET) tool, used for simulating nanoscale devices. This simulator can generate Curves that provide information which engineers can use to explain the physics of Field Effect Transistors (FETs). Moreover, it provides a uniform solution of the equations of Poisson and drift-diffusion (Mustafa et al., 2013). The effects of temperature (from 250 K to 450 K) on three different semiconductor transistors (Si-, Ge-, and GaAs-NWFETs,) were investigated during the simulation. In addition, the channel lengths for the three devices were varied from (25 to 105) nm and the effects of such variations were also investigated. The oxide thickness was fixed at 2.5 nm, while the channel doping concentration was held steady at $1 \times 10^{16} cm^{-3}$ and the drain/source at $1 \times 10^{19} cm^{-3}$. Our simulations involved drain biases ranging from 0.05 V to 1 V and gate biases spanning from 0 V to 1 V. The parameters are listed in the Table below.

Table 1: Parameters Specifications

Parameter	Value
Channel length (Lg)	(25, 45, 65, 85, and 105) nm
Channel diameter (D)	40 nm
Oxide thickness (T_{ox})	2.5 nm
Channel concentration P-type	$10^{16}cm^{-3}$
Channel concentration N-type	$10^{19}cm^{-3}$

In our simulation the I_d-V_g characteristics of NWTs at a temperature (250, 275, 300, 325, 350, 375, 400, 425, and 450 K) were simulated with a channel diameter = 40 nm for different channel length and operating voltages.

RESULTS AND DISCUSSION

The results of the effects of channel length scaling on temperature sensitivity and electrical performance of silicon (Si), germanium (Ge), and gallium arsenide (GaAs) nanowire transistors are presented in this section.

Effect of Temperature on Drain Current at Channel Length of 25 nm

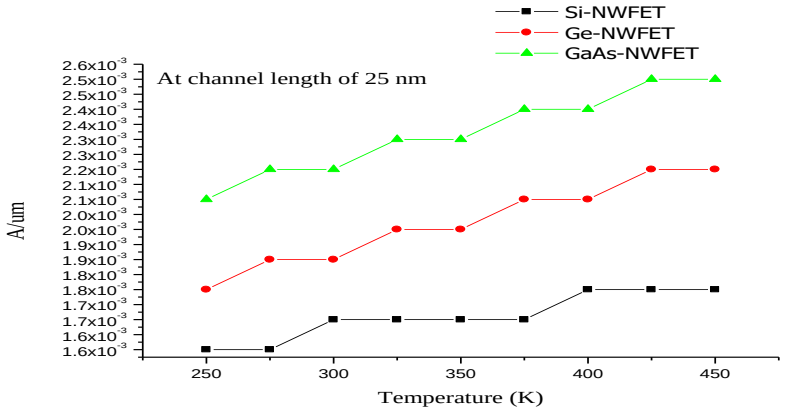

Figure 2: Drain Current Vs Temperature

Figure 2 demonstrates that all nanowire transistors had significant short-channel effects at 25 nm channel length, resulting from aggressive scaling. Si-NWFET, Ge-NWFET, and GaAs-NWFET showed an increase in drain current with increasing temperature from 250 K to 450 K. The lowest drain current of 1.6 × 10^{-3}A/µm for Si-NWFET was observed at 250 – 275 K, this will attribute to lower carrier mobility and higher thermal stability. Ge-NWFET showed moderate current enhancement, which is attributed to the improvement of carrier transport, and GaAs-NWFET, showed the highest drain current, of 2.5 × 10^{-3}A/µm at 450 K, which leads to the improvement of electron mobility and the faster carrier transport capability. The maximum drain current was obtained at 450 K for the three investigated devices. The overall trend was an increase in drain current with temperature, with GaAs-NWFET exhibiting the best performance.

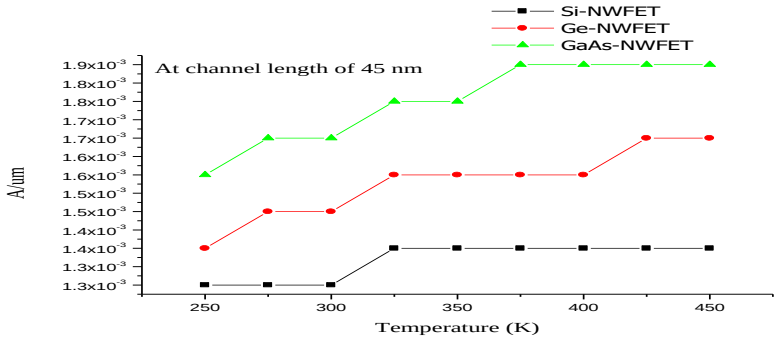

Figure 3 Drain Current Vs Temperature

Effect of Temperature on Drain Current at channel length of 45 nm

Figure 3 shows that all nanowire devices had better electrical stability and less short-channel effects than the 25 nm devices at 45 nm channel length. For the three investigated devices, the drain current rose slowly with temperature from 250 K to 450 K. The lowest drain current of 1.3 × 10^{-3}A/µm was observed at 250 – 300 K for Si-NWFET. Ge-NWFET shows moderate temperature sensitivity and GaAs-NWFET exhibits the highest drain current of 1.9 × 10^{3} A/µm at 375 – 450 K, which is attributed its high carrier mobility. The highest drain current was obtained at 450 K for Si-NWFET, Ge-NWFET and GaAs-NWFET. The trend pattern indicated that the current stability increased as the channel length increased.

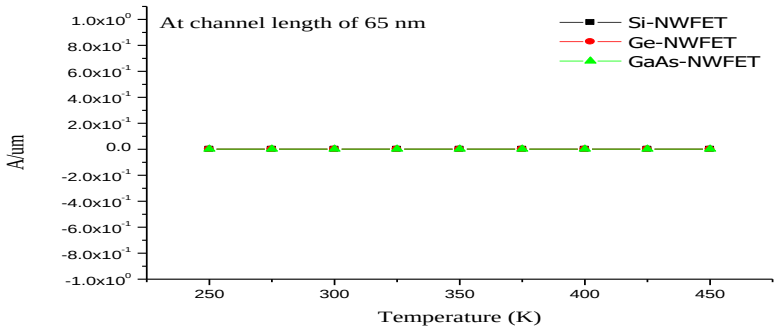

Figure 4 Drain Current Vs Temperature

Effect of Temperature on Drain Current at channel length of 65 nm

The nanowire transistors exhibit superior electrostatic control and thermal stability as shown in Figure 4 at 65 nm channel length. The drain current increased steadily with increasing temperature from 250 K to 450 K for all the three devices. From 250 – 450 K, the Si-NWFET maintained a relatively low and stable drain current of approximately 1.2 × 10^{-3}A/µm, while the Ge-NWFET exhibited moderate current enhancement and the GaAs-NWFET demonstrated the highest drain current of 1.8 × 10^{-3}A/µm at 450 K, due to current conduction capability and reflecting stronger carrier transport. For all the three investigated devices, the maximum drain current was observed at 450 K, The longer-channel devices exhibited reduced leakage current and improved electrical stability, indicating enhanced electrostatic control and reduced short-channel effects.

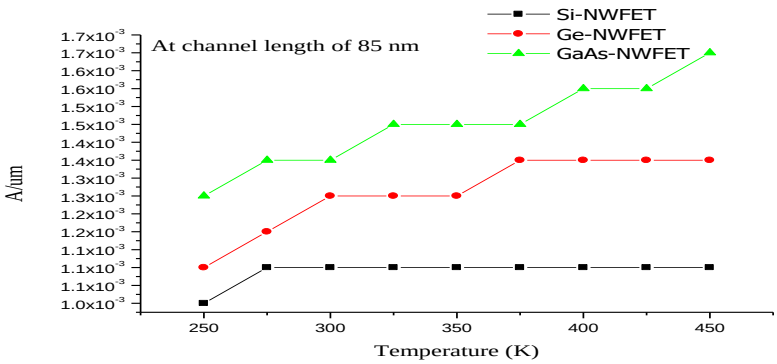

Figure 5: Drain Current Vs Temperature

Effect of Temperature on Drain Current at Channel Length of 85 nm

As can be seen, in Figure 5 all channel materials showed enhanced thermal reliability and stable drain current characteristics at 85 nm channel length. Because of increased carrier excitation, the drain current gradually increased with temperature. The GaAs-NWFET exhibited the highest drain current of 1.7 × 10^{-3}A/µm at 450 K due to its greater carrier mobility, The Si-NWFET exhibited the lowest drain current of 1.0 × 10^{-3}A/µm indicating comparatively lower current-driving capability under the simulated conditions, and Ge-NWFET had moderate current transport. For all the three investigated devices, the maximum drain current happened at 450 K. Smooth variations in drain with temperature and reduce short-channel effects were evident in the trend pattern.

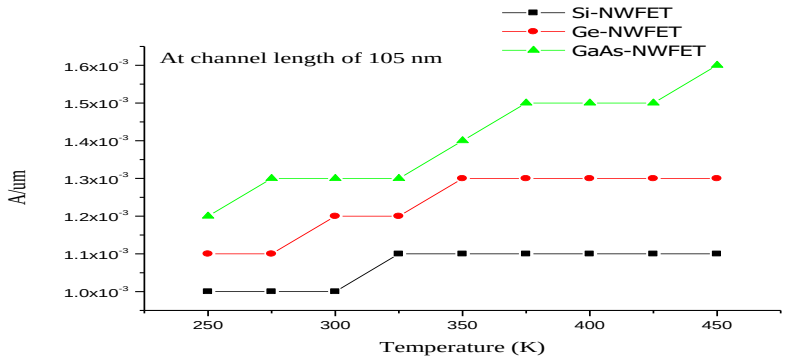

Figure 6: Drain Current Vs Temperature

Effect of Temperature on Drain Current at channel length of 105 nm

The nanowire transistors reached their optimal overall electrical performance at a channel length of 105 nm, as demonstrated in Figure 6 for Si-NWFET, Ge-NWFET, and GaAs-NWFET, the drain current increased steadily with temperature. Ge-NWFET had better carrier transport and stability, Si-NWFET has the lowest drain current of 1.0×10^{-3}µA at 250 – 300 K due to the most stable current characteristics with the least amount of leakage current, and GaAs-NWFET had the highest drain current of 1.6×10^{-3}µA at 450 K due to best overall performance because of its exceptionally high electron mobility. For every device, the maximum drain current happened at 450 K. At longer channel lengths, the trend pattern showed improved electrical stability, decreased DIBL, and excellent electrostatic control.

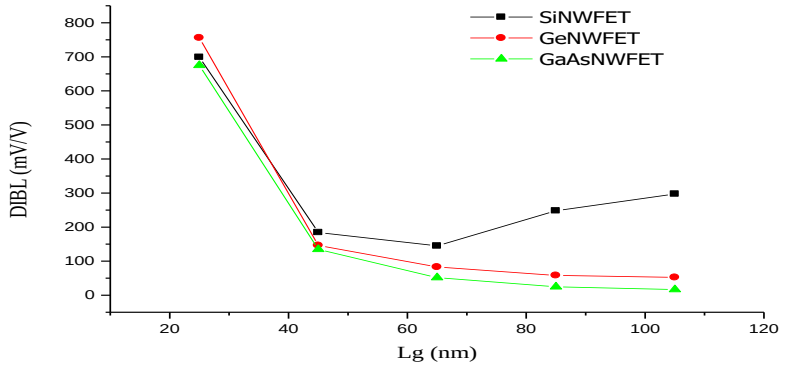

Figure 7 DIBL Vs Channel Length (Lg)

Effect of Channel Length on Drain Induced Barrier Lowering

Figure 7 shows how DIBL for Si-NWFET, Ge-NWFET, and GaAs-NWFET devices varies with channel length. The data show that there is significant reduction in DIBL as the length of the channel increases from 25 nm to 105 nm, indicating that electrostatic control is improved at longer channels, and reduced short-channel effects. The highest DIBL of 756.04mV/V was observed for the Ge-NWFET at 25 nm, indicating strong drain-field influence in the highly scaled device, whereas the lowest value of 16.68mV/V was obtained for the GaAs-NWFET at 105 nm. But at 45 nm, the DIBL values drastically decrease and stabilize. In comparison to Si-NWFET and Ge-NWFET, GaAs-NWFET exhibits slightly reduced DIBL for longer channel lengths, suggesting superior suppression of short-channel effects.

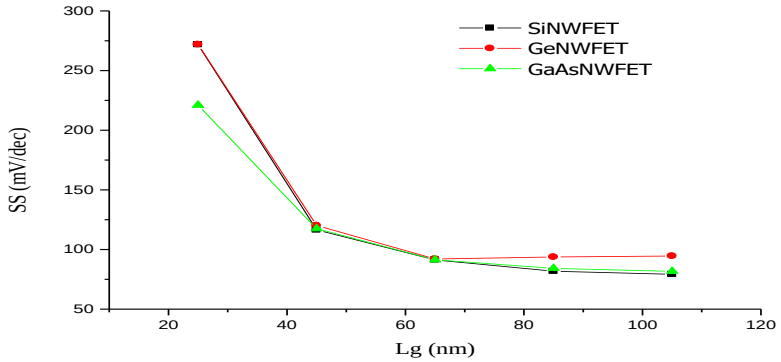

Figure 8: SS Vs Channel Length (Lg)

Effect of Channel Length on Sub Threshold Swing

Figure 8 Enhanced switching properties and decreased short-channel effects at greater channel lengths. All devices exhibit high SS values at 25 nm, which leads to weaker gate control and increased leakage current. The highest SS of 271.92mV/dec was observed for the Ge-NWFET at 25 nm, whereas the lowest value of 79.23mV/dec was obtained for the Si-NWFET at 105 nm. However, for Si-NWFET, Ge-NWFET, and GaAs-NWFET devices, a significant decrease in SS is seen between 45 and 65 nm, following which the subthreshold swing (SS) varies with channel length. As the channel length increases from 25 nm to 105 nm, the data shows that SS drops, indicating that the values become comparatively stable. Compared to Si-NWFET and Ge-NWFET, GaAs-NWFET shows somewhat lower SS values for longer channel lengths, suggesting improved electrostatic control and subthreshold performance.

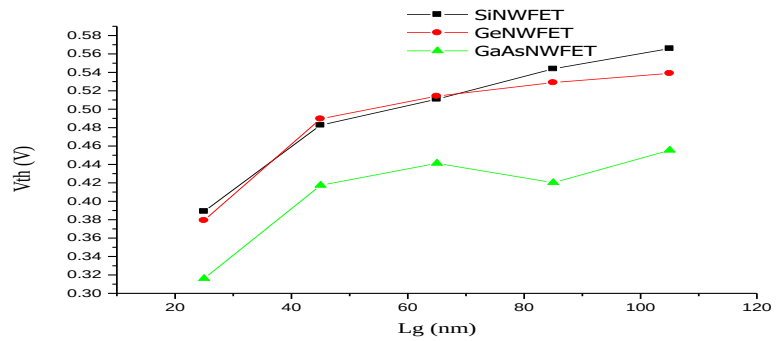

Figure 9 Vth Vs Channel Length (Lg)

Effect of Channel Length on Threshold Voltage

Figure 9 shows how the threshold voltage (Vth) for Si-NWFET, Ge-NWFET, and GaAs-NWFET devices varies with channel length. The findings demonstrate that Vth rises as the length of the channel increases from 25 nm to 105 nm, suggesting better gate regulation and fewer short-channel effects at larger channel lengths. The lower Vth values are observed for the short channel length due to threshold voltage roll-off and also due to the drain effect. Electrostatic integrity improves with an increase in channel length (Vth). The highest Vth value of 0.57 V was observed for Si-NWFET at 25 nm, while the lowest value of 0.316 V was obtained for GaAs-NWFET at 105 nm, the devices with the highest Vth values are Si-NWFET and Ge-NWFET, but GaAs-NWFET has relatively lower Vth values across the channel lengths.

CONCLUSION

This study utilized the MuGFET modeling tool to investigate the effect of channel length scaling on the electrical performance and temperature sensitivity of Si-NWFET, Ge-NWFET, and GaAs-NWFET. The results indicated that, for all devices, the drain current increased with temperature from 250 K to 450 K due to enhanced carrier transport, due to its superior electron mobility, GaAs-NWFET exhibited the highest drain current and optimal electrical performance, while Ge-NWFET produced intermediate results. Si-NWFET had the lowest drain current while providing better thermal stability and lower leakage current. Additionally, the study demonstrated that increasing the channel length from 25 nm to 105 nm reduced short-channel effects, DIBL, and sub threshold swing while improving threshold voltage

stability and electrostatic control. At 450 K and a channel length of 105 nm, all devices exhibited optimal performance. The findings emphasize how important channel length scaling and material selection are for improving nanoscale transistor performance. GaAs-NWFET is suitable for high-speed Nano electronic applications, whereas Si-NWFET is better suited for steady and low-leakage applications. Future research should focus on alternative gate structures, experimental validation, and the use of state-of-the-art semiconductor materials to improve the performance of nanowire transistors.

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